What is claimed is:

What is claimed is:

1. A circuit for converting frequency domain information to time domain information comprising:

a. an Inverse Fast Fourier Transform circuit having a length of N coefficients, the Inverse Fast Fourier Transform circuit adapted to receive input data of length N coefficients and generate output data of length N coefficients that are circularly shifted by m coefficients; and

b. a Cyclical Prefix Insertion circuit adapted to insert a cyclical prefix of length m, the Cyclical Prefix Insertion circuit having;

1. a first switch, connected to the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the Inverse Fast Fourier Transform circuit to an output of the second switch.

2. The circuit for converting frequency domain information to time domain information of claim 1 wherein the N coefficients are modified by a multiplier coupled to the Inverse Fast Fourier Transform circuit, the multiplier adapted to receive the input data and provide the product of the input data and $e^{-j(2*Pi*k*m)/N}$ to the Inverse Fast Fourier Transform circuit.

3. The circuit for converting frequency domain information to time domain information of claim 1 wherein the length of N coefficients is a power of 2 and wherein the Inverse Fast Fourier Transform circuit implements an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms.

4. The circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit, and wherein the N coefficients are modified by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits.

5. The circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, and wherein the N coefficients are modified by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

6. A circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises:

a. a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits and coupled to an input, wherein each butterfly circuit is configured to perform an addition operation and a subtraction operation;

b. a control circuit configured to modify the control to the rotator circuit and to selectively control the plurality of butterfly circuits whether the

addition operation or the subtraction operation is output first in time to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m coefficients; and

c. the contents of the memory of the multiplier circuit with memory are arranged in a suitably modified manner.

7. The circuit for converting frequency domain information to time domain information of claim 3 wherein the length of N coefficients is segmented into first, second, third, and fourth segments of N/4 coefficients, wherein the circular shift m is equal to N/4 and is effected by multiplying the input N coefficients by unity for the first segment of N/4 coefficients, -1 for the second segment of N/4 coefficients, –j for the third segment of N/4 coefficients, and j for the fourth segment of N/4 coefficients.

8. The circuit for converting frequency domain information to time domain information of claim 7 wherein the first, second, third, and fourth segments of N/4 coefficients comprise the length of N coefficients in consecutive order.

9. The circuit for converting frequency domain information to time domain information of claim 7 wherein the N coefficients of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16.

10. The circuit for converting frequency domain information to time domain information of claim 3 wherein the length of N coefficients of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the coefficients at the output of the Inverse Fast Fourier Transform by m coefficients.

11. The circuit for converting frequency domain information to time domain information of claim 10 wherein the N coefficients of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16.

12. The circuit for converting frequency domain information to time domain information of claim 1 wherein the cyclical prefix comprises a guard interval for an orthogonal frequency division multiplexing system.

13. A circuit for converting frequency domain information to time domain information comprising;

a. an Inverse Fast Fourier Transform circuit having:

1. an input adapted to receive frequency domain information;

2. an output providing time domain information;

3. the Inverse Fast Fourier Transform circuit having a length of N coefficients, where N is a power of 2, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the Inverse Fast Fourier Transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, wherein an output of the Inverse Fast Fourier Transform circuit is configured to circularly shift output information by m coefficients, where m is less than N; and

b. guard interval insertion circuit adapted to insert a cyclical prefix of length m, the guard interval insertion circuit having;

1. a first switch, connected to the output of the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the output of the Inverse Fast Fourier Transform circuit to an output of the second switch.

14. The circuit for converting frequency domain information to time domain information of claim 13 wherein the Inverse Fast Fourier Transform circuit is configured to circularly shift output information by m coefficients by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

15. The circuit for converting frequency domain information to time domain information of claim 13 wherein the Inverse Fast Fourier Transform circuit is configured to circularly shift output information by m coefficients by modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits.

16. The circuit for converting frequency domain information to time domain information of claim 13 wherein the length of N coefficients of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the Inverse Fast Fourier Transform circuit to circularly shift the output data by 16 coefficients.

17. A circuit for converting frequency domain information to time domain information comprising:

a. a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift is approximately the same as a desired cyclical prefix;

b. a first switch, connected to the means for performing a circularly rotated Inverse Fast Fourier Transform;

c. a means for buffering a portion of the time domain signals approximately the same as the desired cyclical prefix, the means for buffering having an input connected to the first switch; and

d. a second switch, coupled to the first switch and to the means for buffering, wherein the first and second switches selectively couple the output of the means for buffering and the means for performing a circularly rotated Inverse Fast Fourier Transform circuit to an output of the second switch.

18. The circuit for converting frequency domain information to time domain information of claim 17 wherein the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for multiplying input data by $e^{-j(2*Pi*k*m)/N}$.

19. The circuit for converting frequency domain information to time domain information of claim 17 wherein the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

20. The circuit for converting frequency domain information to time domain information of claim 17 wherein the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying the order of the

contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits.

21. The circuit for converting frequency domain information to time domain information of claim 17 wherein the cyclical prefix comprises a guard interval for an orthogonal frequency division multiplexing system.

22. A method of generating circularly shifted time domain signal from frequency domain information in an Inverse Fast Fourier Transform circuit and having a desired cyclical prefix comprising:

a. performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the amount of the circular shift is the same as the length of the cyclical prefix;

b. storing the time domain information for a number of clock cycles equal to the cyclical prefix in a buffer while simultaneously outputting the time domain information;

c. outputting the time domain information for a number of clock cycles equal to a length of the Inverse Fast Fourier Transform minus the length of the cyclical prefix; and

d. outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix.

23. The method of claim 22 wherein the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises a step of multiplying input data by $e^{-j(2*Pi*k*m)/N}$.

24. The method of claim 22 wherein the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

25. The method of claim 22 wherein the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises modifying the order of the contents of the memory and modifying the control of the rotator circuits and butterfly circuits.

26. A circuit for converting between frequency domain information and time domain information comprising a transform circuit having a length of N coefficients, where N is a power of 2, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, wherein an output of the transform circuit is circularly shifted by m coefficients by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N.

27. The circuit of claim 26 wherein the transform circuit comprises a Fast Fourier Transform circuit.

28. The circuit of claim 26 wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit.

29. The circuit of claim 26 wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m coefficients.

30. A circuit for converting between frequency domain information and time domain information comprising a transform circuit having a length of N coefficients,

where N is a power of 2, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, wherein an output of the transform circuit is circularly shifted by m coefficients by modifying the control to the butterfly circuit, modifying the control to the rotator circuit and re-ordering the memory contents of the multiplier circuit, where m is less than N.

31. The circuit of claim 30 wherein the transform circuit comprises a Fast Fourier Transform circuit.

32. The circuit of claim 30 wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit.

33. The circuit of claim 30 wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m coefficients.